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PATENTS

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In re application of

Hirokazu HONDA

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GROUP 2827

Examiner D. Graybill



MULTILAYER INTERCONNECTION BOARD, SEMICONDUCTOR DEVICE HAVING THE SAME, AND METHOD OF FORMING THE SAME AS WELL AS METHOD OF MOUNTING THE SEMICONDUCTOR CHIP ON THE INTERCONNECTION BOARD

**AMENDMENT**

Commissioner for Patents

Washington, D.C. 20231

Sir:

Responsive to the Official Action of March 5, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Amend claim 1 as follows:

--1. (amended) A semiconductor device comprising:

an interconnection board having first and second surfaces; and

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a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board,

said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board.-

Amend claim 8 as follows:

--8. (amended) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one semiconductor chip mounted on said first surface of said interconnection board; and

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a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board,

said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least processes for manufacturing said interconnection board and for mounting said at least one semiconductor chip on said first surface.--

Amend claim 18 as follows:

--18. (amended) A semiconductor device comprising:

an interconnection board having first and second surfaces;

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at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board; and

a buffer layer having a first surface in contact with said second surface of said interconnection board and also said buffer layer having a second surface on which at least one external electrode is provided, and said buffer layer providing at least one electrical contact between said one external electrode pad and said at least one external electrode, and said buffer layer being capable of absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.--

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Amend claim 37 as follows:

--37. (amended) The semiconductor device as claimed in claim 36, wherein said supporting layer further comprises:

a supporting plate having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer; and

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a supporting sealing resin material filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.--

[Amend claim 38 as follows:]

--38. (amended) The semiconductor device as claimed in claim 18, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.--

Amend claim 43 as follows:

--43. (amended) A semiconductor device comprising:

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an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board;

at least one external electrode fixed to said at least one external electrode pad; and

a supporting layer on said second surface of said interconnection board for supporting said external electrodes.--

[Amend claim 44 as follows:]

--44. (amended) The semiconductor device as claimed in claim 43, further comprising:

a buffer layer having a first surface in contact with said second surface of said interconnection board, and

wherein said supporting layer further comprises

a supporting plate having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer; and

a supporting sealing resin material filling said inter-

space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.--

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[Amend claim 45 as follows:]

--45. (amended) The semiconductor device as claimed in claim 43, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.--

Amend claim 49 as follows:

--49. (amended) The semiconductor device as claimed in claim 48, further comprising:

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a buffer layer having a first surface in contact with said second surface of said interconnection board;

a stiffener extending on a peripheral region of said buffer layer; and

at least a heat spreader provided on said at least semiconductor chip and on said stiffener.--

Please add the following new claims:

--80. (new) A semiconductor device comprising:

an interconnection board having first and second surfaces;

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at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane; and

a high rigidity plate securely fixed to and directly contact with at least a majority of said single flat plane,

said high rigidity plate being higher in rigidity than said interconnection board and suppressing said interconnection board from being bent.

--81. (new) The semiconductor device as claimed in claim 80, wherein said high rigidity plate is securely fixed to and directly in contact with an entirety of said single flat plane.

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--82. (new) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board; and

a high rigidity plate securely fixed to and directly contact with at least a majority of said single flat plane,

said high rigidity plate being higher in rigidity than said interconnection board and suppressing said interconnection board from being bent.

--83. (new) The semiconductor device as claimed in claim 82, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said single flat plane.

--84. (new) The semiconductor device as claimed in claim 1, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.

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--85. (new) The semiconductor device as claimed in claim 8, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.--

Please charge the fee of $84 for the extra independent claim added herewith, to Deposit Account No. 25-0120.

REMARKS

The case has been amended to be in condition for allowance.

Claims 1-59 are pending, together with newly-added claims 80-85. Claims 1, 8, 18, 43, 80, and 82 are independent.

The Official Action rejected claims 37, 38-42, and 44-49 under §112, second paragraph, as indefinite.

Claim 37 has been amended to depend from claim 36. Claim 36 provides the antecedent basis for "said supporting layer".

Claims 38 and 45 have been amended to recite the chip being bonded to the "first" surface of the board.

Claims 44 and 49 have been amended to recite "the buffer layer" as a further included feature.

In view of the above, withdrawal of the indefiniteness rejection is solicited.

There are no other formal matters outstanding.

Claims 1-3, 5-10, 12-17 are rejected as anticipated by TSUKAMOTO 5,841,194; claims 1, 4, 8, and 11 as anticipated by FARQUHAR 6,329,713; and claims 18-36, 38-43, 45-48, and 50-59 as anticipated by ALLEN 4,705,205.

The Official Action is somewhat unclear. It appears that at the bottom of page 13, that claims 19, 21, 38-42, 45-48, and 54 are rejected as obvious over ALLEN in view of TSUKAMOTO as it is admitted that ALLEN does not disclose all the features of these claims.

Claims 37, 44, and 49 were not substantively rejected, but were also not indicated to include allowable subject matter.

The independent claims, as amended, as well as the new claims, are believed to patentably recite the present invention.

The present invention provides an interconnection board that remains securely fixed to a high rigidity plate. The plate thereby suppresses the interconnection board from being bent under application of any stress and/or strain during the manufacturing process.

Claims 1-17

Claims 1-17 are directed to an intermediate product which, as recited, includes the interconnection board and the high rigidity plate securely fixed to the interconnection board

for suppressing the interconnection board from any bending due to application of any stress and/or strain during the manufacturing process.

After the interconnection board has been completed, the high rigidity plate may be removed or may be processed to other elements such as the buffer layer as illustrated in the drawings attached to the present application.

None of the applied prior art references teach or suggest the recited inventive combination.

Indeed, none of the applied prior art references disclose the intermediate product including the interconnection board and the high rigidity plate.

At best, what is disclosed in or taught by the applied references, alone or in combination, is a structure which may provide that at most a minority part of the interconnection board including pads is connected to a high rigidity plate. As the claims have been amended, these references neither anticipate nor render obvious the recited invention.

See in fact that the applied structures disclose to ensure that the majority part of the second surface of the interconnection board are slightly distanced from, or are not fixed to, the high rigidity plate.

TSUKAMOTO

TSUKAMOTO does disclose that a peripheral stiffener 106 (high rigidity plate) is fixed to only a peripheral part--but

this is only a minority part--of a second surface of a flexible carrier substrate 108 (interconnection board) as shown in FIGS. 1, 2, 4-6, and 8-10.

The carrier substrate as the final product of "carrier substrate" includes the flexible substrate with the peripheral stiffener. For the flexible substrate, the stiffener is needed to keep the general shape of "flatness" of the substrate as the final product.

In contrast, the present invention does not require the interconnection board, as the final product does not need any high rigidity plate such as stiffener. The role of the high rigidity plate in accordance with the present invention is never required to support the general shape of the final product, but is to suppress the interconnection board from any small bending due to application of any stress and/or strain during the manufacturing process, in order to obtain a desired interconnection board free of any small bend, thereby allowing highly accurate lithography processes and a highly reliable bonding between the board and the chip.

Thus, the nature of the rigid plates in the present invention and in the prior art is very different. Accordingly, the manner in which the rigid plates are attached are also different. The prior art does not anticipate nor render obvious the presently-recited invention as the plates of the prior art serve a different purpose and are attached differently.

For example, common to all of the preferred embodiments of the present invention, the entirety of the second surface of the interconnection board including pads is flat and in contact securely and directly with the high rigidity plate for suppressing the interconnection board from any small bend due to application of any stress and/or strain during the manufacturing process.

FARQUHAR

FARQUHAR discloses that the laminate circuit element 1 (interconnection board) is joined to a stiffener 8 (high rigidity plate) by a bonding film 9 which has an adhesive on both surfaces. The stiffener 8 is in contact securely and directly with the bonding film 9 but never the stiffener 8 (high rigidity plate). Further, the stiffener 8 (high rigidity plate) is present in the final product, the stiffener 8 (high rigidity plate) acting as a heat sink and a heat spreader (on column 5, lines 24-26). For this reason, the final product needs the stiffener 8 (high rigidity plate).

By contrast to FARQUHAR, in accordance with the present invention, the interconnection board (in the final product) does not need any high rigidity plate as a stiffener is no longer needed.

No high rigidity plate in the present invention is needed to support the general shape of the final product. The present invention, however, does note a structure with a rigidity plate, but the plate is to suppress the interconnection board from any small bend due to application of any stress and/or

strain during the manufacturing process.

Further, in accordance with the present invention, no film nor other layer is interposed between the interconnection board and the high rigidity plate. Namely, commonly to all of the preferred embodiments of the present invention, the entirety of the second surface of the interconnection board including pads is flat and in contact securely and directly with the high rigidity plate.

The intermediate product claims 1-17 include two independent claims 1 and 8.

The remaining claims

The remaining product claims 18-59 are directed to the final product which includes the interconnection board, but without the high rigidity plate.

Although, the above-described feature of the present invention concerning the rigidity plate does not directly appear on the final product, it may appear indirectly on the following structure of the final product.

In accordance with the final product of the present invention, the entirety of the second surface of the interconnection board including pads should be flat for allowing the entirety of the second surface to be in contact securely and directly with the high rigidity plate for suppressing the interconnection board from any small bend due to application of any stress and/or strain during the manufacturing process.

Surfaces of pads should be leveled to the second surface of the interconnection board. That is, the entirety of the second surface, including the electrode pads, of the interconnection board should be flat.

ALLEN was offered as anticipating claims 18-36, 38-43, 45-48, and 50-59.

ALLEN discloses that a chip carrier 32 is connected to a circuit board through a plurality of preforms or solder columns 28, 48, 54, 56, 60, 62, 72, 82, 91 and 95 (buffer layer) as shown in Figures 7, 8, 10, 11, 12, 13, and 14. ALLEN also discloses that a chip device 10 is connected to a circuit board 12 through a solder column 18 (buffer layer).

Accordingly, what is **taught** by ALLEN is that the buffer layer is interposed between the semiconductor chip and the interconnection board for absorbing and/or relaxing a stress applied to between the semiconductor chip and the interconnection board. Note, however, that the retaining member 22/58 **does not** correspond to the buffer layer which absorbs and/or relaxes a stress applied to between the semiconductor chip and the interconnection board, because the retaining member 22/58 surrounds and retains the buffer layer (the plurality of preforms or solder columns 28, 48, 54, 56, 60, 62, 72, 82, 91 and 95) for absorbing and/or relaxing a stress applied to between the semiconductor chip and the interconnection board. In addition, the retaining member 22/58 is also interposed between the semiconductor chip and the interconnection board.

Further, the Official Action stated that the retaining member 22 corresponds to the supporting layer. The supporting layer comprising the retaining member 22 is to support the buffer layer (the plurality of preforms or solder columns 28, 48, 54, 56, 60, 62, 72, 82, 91 and 95).

In contrast to ALLEN, in accordance with the final product of the present invention as recited in independent claim 18, the interconnection board is interposed between the semiconductor chip and the buffer layer, and the buffer layer is interposed between the interconnection board and the at least one external electrode for absorbing and/or relaxing a stress applied to between the interconnection board and the at least one external electrode.

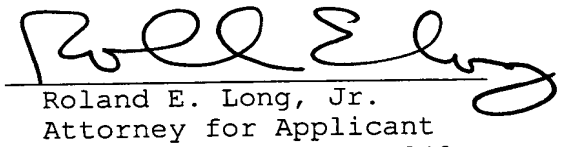
Accordingly, the ALLEN anticipation rejection is not believed to be viable.

Reconsideration and allowance of all the pending claims is respectfully requested.

A marked-up copy of the amended claims is attached.

Respectfully submitted,

YOUNG & THOMPSON

By 

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